WHAT IS CLAIMED IS:

1. A clock-synchronizing apparatus of devices with different clocks comprising:

a first device operated according to a first clock and generating control signals at a speed of a second clock;

a second device operated by being synchronized with the second clock according to the control signals and having an operation latency of one clock period of the first clock; and

a clock driver generating the second clock by multiplying the first clock by predetermined even times and removing a phase delay between the second clock and the first clock.

2. The apparatus of claim 1, wherein the predetermined even times includes double and a clock ratio of the first clock and second clock includes 1:2.

3. The apparatus of claim 2, wherein the first device can generate control signals at the speed of the second clock by using the first clock and a clock shifted as long as a 1/4 clock period of the first clock.

4. The apparatus of claim 1, wherein the second device delays an operation timing by one clock period according to a control signal for performing a clock suspension function among the control signals.

5. The apparatus of claim 1, wherein the first device comprises a microprocessor, the second device comprises a RAM, and the predetermined even times comprises double.

6. The apparatus of claim 5, wherein the microprocessor includes a memory controller of which a RAM control signal generation method can be programmed by a user, and wherein the memory controller can generate the control signals at the speed of the second clock.

7. The apparatus of claim 6, wherein the RAM delays its operation timing by one clock period according to a control signal performing the clock suspension function among the generated control signals.

8. The apparatus of claim 7, wherein an enable period of the control signal performing the clock suspension function has a 1/4 clock period of the first clock.

9. A clock-synchronizing method of devices with different clocks comprising:

programming a generation interval of RAM control signals so as to correspond to an operation latency of a RAM, that interfaces between a microprocessor and the RAM which has a speed of predetermined even times a speed of a microprocessor clock;

generating the RAM control signals corresponding to a specific operation mode at a speed of a RAM clock according to the programmed generation interval and outputting the RAM control signals from the microprocessor to the RAM; and

performing an operation according to the operation mode between the microprocessor and the RAM on the basis of the microprocessor clock by the RAM control signals generated at the speed of the RAM clock according to the programmed generation interval.

10. The method of claim 9, wherein a ratio of the microprocessor clock and the RAM clock includes 1:2.

11. The method of claim 9, wherein the operation latency of the RAM is equal to one clock period of the microprocessor clock.

12. The method of claim 9, wherein an enable period of the generated RAM control signals is equal to a 1/4 clock period of the microprocessor clock.

13. The method of claim 9, wherein the specific operation mode comprises:

a mode reading a data from the RAM by the microprocessor;

a mode writing a data to the RAM by the microprocessor;

a mode refreshing the RAM; and

a mode setting a mode of the RAM.

14. The method of claim 9 further comprising:

programming an RCD (RAS to CAS Delay) of the RAM as one clock period of the microprocessor clock, if the specific operation mode is the read mode of the microprocessor;

programming a CL (CAS Latency) of the RAM as one clock period of the microprocessor clock;

programming an enable period of the RAM control signal to perform the clock suspension function as a 1/4 clock period of the microprocessor clock; and

programming an RP (precharge time) to precharge the RAM as one clock period of the microprocessor clock.

15. The method of claim 14 further comprising:

outputting data during two clock periods of the RAM clock from the RAM, when the RAM control signal performing the clock suspension function is enabled.

16. The method of claim 9 further comprising if the specific operation mode is a burst write mode of the microprocessor:

an operation in which the RCD of the RAM is programmed as one clock period of the microprocessor clock;

an operation in which the CL of the RAM is programmed as one clock period of the microprocessor clock;

an operation in which an enable period of the RAM control signal for performing the clock suspension function is programmed to be a 1/4 clock period of the microprocessor;

an operation in which the RAM control signal is programmed to be enabled at each microprocessor clock until one period of the burst write is finished; and

an operation in which the RP that precharges the RAM is programmed to be one clock period of the microprocessor.

17. The method of claim 16, wherein when the RAM control signal is enabled, the data input operation of the RAM is delayed by each one clock period of the RAM clock.

18. A clock-synchronizing method of devices with different clocks comprising:

programming memory control signals so as to correspond to an operation latency of a memory interfacing between a microprocessor and the memory that has a speed of predetermined even times a speed of a microprocessor clock;

generating the memory control signals corresponding to a specific operation mode at a speed of a memory clock according to the programmed memory control signals and outputting the memory control signals from the microprocessor to the memory; and

performing an operation according to the operation mode between the microprocessor and the memory on the basis of the microprocessor clock by the memory control signals generated at the speed of the memory clock according to the programmed generation interval.

19. The method of claim 18, wherein a ratio of the microprocessor clock and the memory clock includes 1:2.

20. The method of claim 18, wherein the operation latency of the memory is equal to one clock period of the microprocessor clock.

21. The method of claim 18, wherein an enable period of the generated memory control signals equals to a 1/4 clock period of the microprocessor clock.

22. A clock-synchronizing method of devices with different clocks comprising:

performing a read operation of a microprocessor according to a clock suspension function of a RAM;

outputting a clock enable signal from the microprocessor according to a clock suspension function of RAM; and

using an internal clock signal of the RAM and suspending RAM operation for at least one clock according to the clock enable signal and wherein the RAM maintains a data outputting by as long as one more clock period.

23. The method of claim 22 further comprising:

the RAM outputting data for every one clock period of the microprocessor and the microprocessor can read outputted data at every one clock period of the microprocessor.

24. The method of claim 22 further comprising:

during a microprocessor write operation to the RAM, a clock suspension function is applied wherein the microprocessor outputs a clock enable signal to the RAM and the RAM waits for data inputting for at least one clock period and receives data at a rising edge of the next clock period.

25. A clock-synchronizing method of devices with different clocks comprising:

outputting a clock enable signal from a microprocessor to a RAM;

suspending an internal clock signal of the RAM for at least one clock period according to the clock enable signal; and

wherein the RAM waits for data inputting for at least one clock period and receives a data from the microprocessor at a rising edge of the next clock period.

26. The method of claim 25, wherein the microprocessor outputs data at every two clock periods of the RAM and the RAM can receive the data from the microprocessor at every two clock periods.

27. The method of claim 25, wherein RAM signal information is stored in a memory control table of the microprocessor and at least one signal of the signal information corresponds to one clock period of the microprocessor and the at least one signal of the signal information is enabled for a ¼ clock period of the microprocessor.